REMARKS

The Office Action mailed February 25, 2003 has been reviewed and the comments of the Patent and Trademark Office have been considered. Claims 1-11, 15-21, 23, and 25-33 were pending in the application. Claims 1, 4, 11, 15, 23, 32, and 33 are amended, no claims have been cancelled and claims 34 and 35 are newly added. Therefore, claims 1-11, 15-21, 23, and 25-35 are pending in the application.

FIG. 3 has been amended as shown in red on the drawings attached to the Proposed Changes to the Drawings being filed concurrently herewith.

Claim 33 is rejected under 35 U.S.C. § 112, first paragraph, as allegedly containing subject matter that is not described in the specification. However, the originally filed specification describes the recited claim limitation almost verbatim. For example, page 16, lines 17-25 describes "The element isolation region 2 is formed by the STI (Shallow Trench Isolation)...." Furthermore, the previous paragraph (page 16, lines 10-16) clarifies that the n-channel IGFET is formed on a main surface of a P-well region that is *surrounded* by the element isolation region 2. Accordingly, claim 33 fully complies with the requirements of 35 U.S.C. § 112, first paragraph, and this rejection should be withdrawn.

In the Office Action, claims 1-11, 15-21, 23, and 25-32 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. patent 5,583,059 to Burghartz (hereafter "Burghartz") and U.S. patent 5,241,214 to Herbots et al. (hereafter "Herbots"). Claim 33 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Burghartz and Herbots in further view of U.S. patent 5,357,119 to Wang et al. (hereafter "Wang"). Applicants respectfully traverse these rejections for at least the following reasons.

Each of the pending independent claims recite, *inter alia*, the structure of the gate electrode being formed on a gate insulating film with a first region including a first group IV element and a second group IV element formed in contact with the insulating gate film while a second region including the first group IV element is formed on the insulating gate film via the first region. Neither the structure nor the purpose of the claimed invention is disclosed or suggested by the applied prior art.

For example, with respect to claim 1, the Office Action acknowledges that Burghartz does not disclose the claimed channel forming region between a pair of main electrodes

(although the Office Action states that this would be inherent). Thereafter, the office action relies on Herbots for disclosing a channel region between a source and drain for completing a FET as disclosed in Burghartz. (It should be noted that Burghartz does not disclose or suggest the claimed *gate* electrode structure formed on the insulating gate film and therefore Herbots does not cure the deficiencies of Burghartz.)

Referring to the cited Fig. 2A of Burghartz, the silicide contact 10A is in contact with the SiGe base layer 5. Furthermore, Fig. 1 of Burghartz discloses that the silicide contact 10A reaches the collector region (Si layer) 4 via the SiGe base layer 5. Therefore, Burghartz teaches that it is acceptable that Ge gets mixed into the silicide contact 10A.

In sharp contrast, the pending independent claims recite that the second region (Si) is provided between the first region (SiGe) and, for example, the silicide layer in order to prevent Ge from being mixed in the silicide layer. That is, both the structure and purpose of the claimed invention is different from that disclosed in the applied prior art.

New claims 34 and 35 also recite similar features to that recited in the earlier pending claims from a slightly different perspective and are also believed to be condition for allowance for reasons that are similar to that discussed above.

The dependent claims are also patentable for at least the same reasons as the independent claims on which they ultimately depend. In addition, they recite additional patentable features when considered as a whole.

In view of the foregoing, applicants believe that the application is in condition for allowance and entry and reconsideration is respectfully requested If there are any questions regarding the application or if an examiner's amendment would facilitate the allowance of one or more of the claims, the examiner is invited to contact the undersigned attorney at the local telephone number below.

Respectfully submitted,

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May 27, 2003 (Tuesday after holiday)
Date

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Attached: Attachment A

Should additional fees be necessary in connection with the filing of this paper, or if a petition for extension of time is required for timely acceptance of same, the Commissioner is hereby authorized to charge deposit account No. 19-0741 for any such fees; and applicants hereby petition for any needed extension of time.

ATTACHMENT A

Marked up version of claim amendments made in the Amendment filed May 27, 2002

1. (Five Times Amended) A semiconductor device comprising:

a pair of main electrodes used as source and drain electrodes;

a channel forming region provided between the pair of main electrodes;

an insulating gate film formed on the channel forming region; and

a gate electrode formed on the insulating gate film, and provided with a first region including [at least] a first group IV element and a second group IV element and formed in contact with the insulating gate film, and a second region including the first group IV element and formed on the insulating gate film via the first region, the first and second regions having an identical conductivity type.

4. (Five Times Amended) A semiconductor device comprising:

an insulated gate field effect transistor having a pair of main electrodes used as source and drain electrodes, a channel forming region provided between the pair of main electrodes, an insulating gate film formed on the channel forming region, and a gate electrode formed on the insulating gate film, and provided with a first region including [at least] a first group IV element and a second group IV element and formed in contact with the insulating gate film, and a second region including the first group IV element and formed on the insulating gate film via the first region, the first and second regions having an identical conductivity type; and

a silicide electrode formed in contact with the second region of the gate electrode, and being substantially free from the second group IV element.

11. (Five Times Amended) A semiconductor device comprising:

an insulated gate field effect transistor having a pair of main electrodes used as source and drain electrodes, a channel forming region provided between the pair of main electrodes, an insulating gate film formed on the channel forming region, and a gate electrode formed on

the insulating gate film, and provided with a first region including [at least] a first group IV element and a second group IV element and formed in contact with the insulating gate film, and a second region including a multiple element compound including [at least] the first and second group IV elements and metal, and formed on the insulating gate film via the first region, the first and second regions having an identical conductivity type; and

a silicide electrode formed in contact with the second region of the gate electrode, including the first group IV element and metal, and being substantially free from the second group IV element.

15. (Four Times Amended) A semiconductor device comprising:

a semiconductor region of a first conductivity type;

an epitaxial growth layer formed on the semiconductor region and having a first region of the first conductivity type including [of at least] a first group IV element and a second group IV element and formed in contact with the semiconductor region, and a second region of the first conductivity type including [of] the first group IV element and formed [in contact with] on the semiconductor region via the first region; and

a silicide electrode formed on the second region of the epitaxial growth layer.

23. (Five Times Amended) A semiconductor device comprising:

an insulated gate field effect transistor having a pair of main electrodes used as source and drain electrodes, a channel forming region provided between the pair of main electrodes, an insulating gate film formed on the channel forming region, and a gate electrode formed on the insulating gate film, and provided with a first region including [at least] a first group IV element and a second group IV element and formed in contact with the insulating gate film, and a second region including the first group IV element and formed on the insulating gate film via the first region, the first and second regions having an identical conductivity type;

[a respective] an elevated electrode formed on the main electrodes, and having a third region including a third group IV element and a fourth group IV element and a fourth region formed on the main electrode via the third region and including the third group IV element;

a first silicide electrode formed in contact with the second region of the gate electrode, and being substantially free from the second group IV element; and

a second silicide electrode formed in contact with the fourth region of the elevated electrode, and being substantially free from the fourth group IV element.

32. (Amended) A semiconductor device comprising:

a first conductivity type insulated gate field effect transistor having a pair of first conductivity type main electrodes used as source and drain electrodes, a second conductivity type channel forming region provided between the pair of first conductivity type main electrodes, a first insulating gate film formed on the second conductivity type channel forming region, and a first gate electrode formed on the first insulating gate film, and provided with a first region including [at least] a first group IV element and a second group IV element and formed in contact with the first insulating gate film, and a second region including the first group IV element and formed on the first insulating gate film via the first region, the first and second regions having an identical conductivity type; and

a second conductivity type insulated gate field effect transistor having a pair of second conductivity type main electrodes used as source and drain electrodes, a first conductivity type channel forming region provided between the pair of second conductivity type main electrodes, a second insulating gate film formed on the first conductivity type channel forming region, and a second gate electrode formed on the second insulating gate film, and provided with a third region including [at least] the first group IV element and the second group IV element and formed in contact with the second insulating gate film, and a fourth region including the first group IV element and formed on the second insulating gate film via the third region, the third and fourth regions having [an] the identical conductivity type.

33. (Amended) A semiconductor device comprising:

an insulated gate field effect transistor having a pair of main electrodes used as source and drain electrodes, a channel forming region provided between the pair of main electrodes, an insulating gate film formed on the channel forming region, and a gate electrode formed on the insulating gate film, and provided with a first region including [at least] a first group IV

element and a second group IV element and formed in contact with the insulating gate film, and a second region including the first group IV element and formed on the insulating gate film via the first region, the first and second regions having an identical conductivity type; and

an element isolation region formed surrounding the insulated gate field effect transistor, and having an insulating film embedded in a trench.

~~Fig.3~~

FIG. 3 (A)

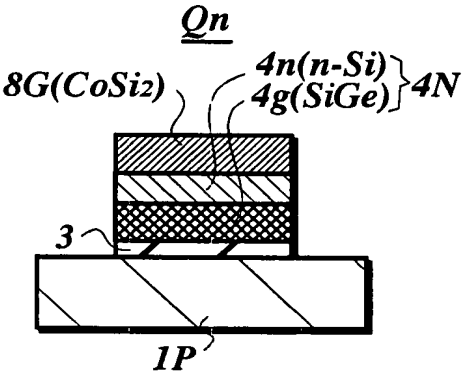

FIG3 (B)

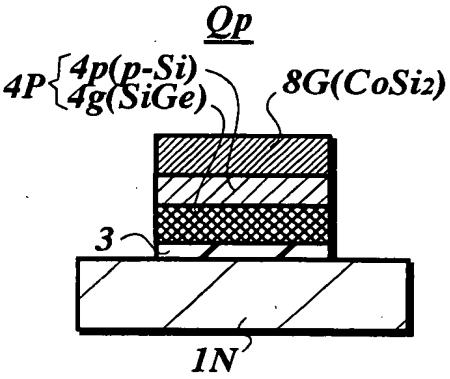

Fig.4